SYSTEM AND METHOD FOR INTERLEAVING SDRAM DEVICE ACCESS REQUESTS

Abstract of the Disclosure

A method and system is provided for interleaving multiple cycles streams from clients seeking SDRAM access. More particularly, a master scoreboard register is established for enabling the interleaving of many clients SDRAM access requests into a single stream optimized for maximum packing density of the different streams, thereby reducing the overhead associated with each individual stream. In one embodiment, at least one Master Score Board Register (MSBR) is provided for storing the order of cycles to go out of a controller/processor and to the SDRAM. If there is a set bit in a particular location in the MSBR then it means that the cycle is occupied and already allocated and cannot be used for anything else. If the bit is not set then the cycle that bit represents a vacant slot ready for use by a client. Upon receipt of an SDRAM request, an interleaving engine identifies the bit locations in the MSBR associated with the requested cycles. It is then determined whether any of the requested bits are spoken for in the MSBR. If so, the client's command sequence is rejected for at least the present clock cycle and the MSBR is incremented and the requested bits are checked again during the next clock cycle.